

Low Power, Precision FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

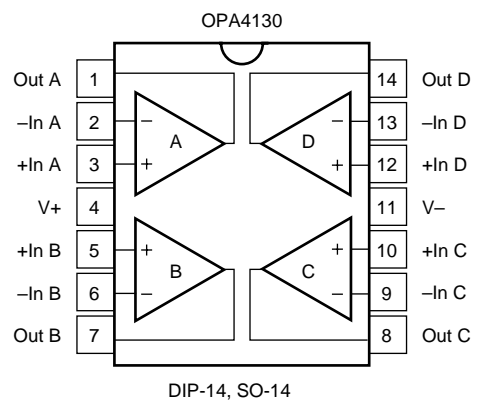
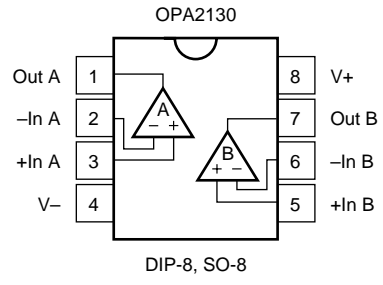
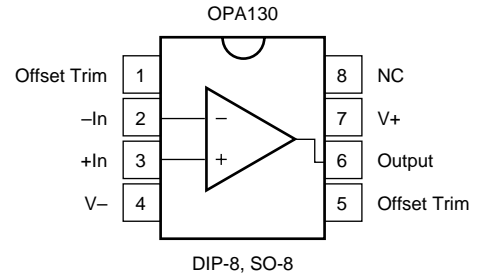
- **LOW QUIESCENT CURRENT:** 530 μ A/amp
- **LOW OFFSET VOLTAGE:** 1mV max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH CMRR:** 90dB min
- **FET INPUT:** $I_B = 20$ pA max
- **EXCELLENT BANDWIDTH:** 1MHz
- **WIDE SUPPLY RANGE:** ± 2.25 to ± 18 V
- **SINGLE, DUAL, AND QUAD VERSIONS**

DESCRIPTION

The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in DIP-8 and SO-8 surface-mount packages. Quad is available in DIP-14 and SO-14 surface-mount packages. All are specified for -40°C to $+85^\circ\text{C}$ operation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	36V
Input Voltage	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit ⁽²⁾	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

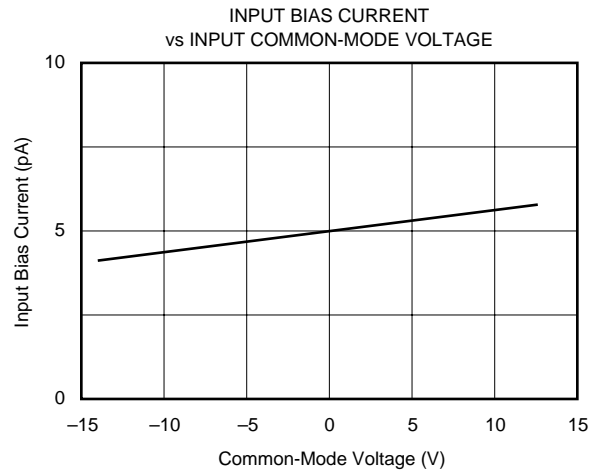
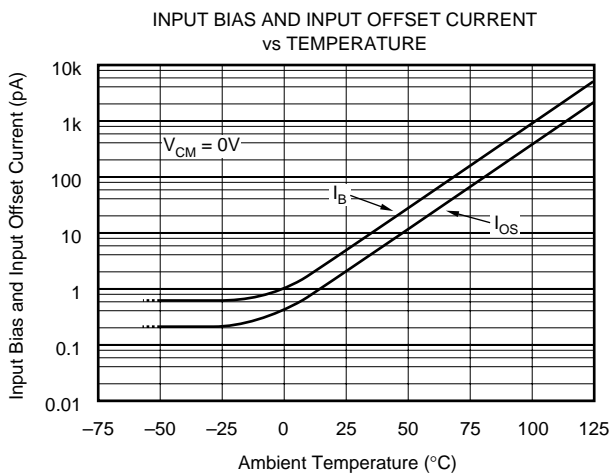
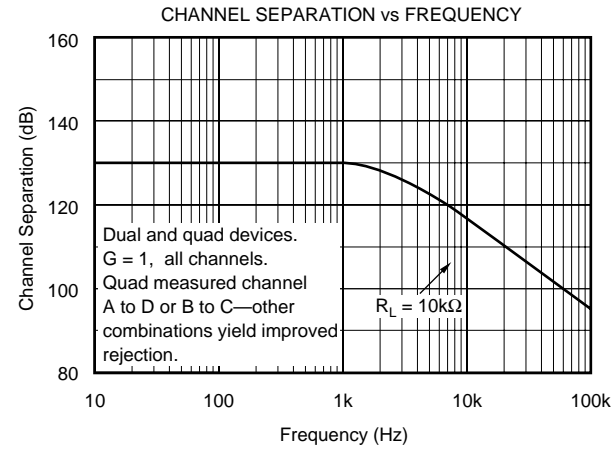
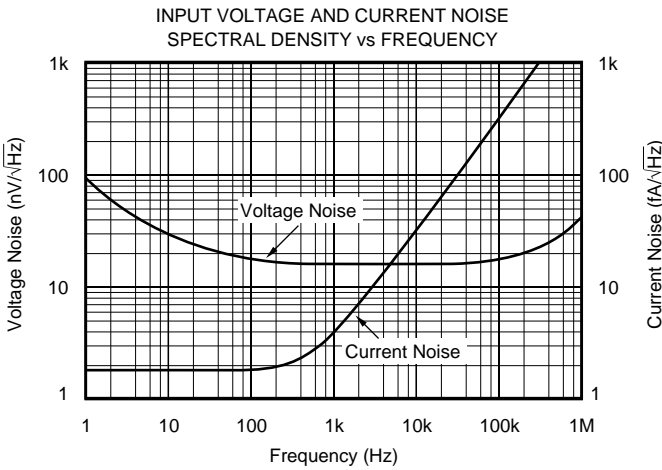
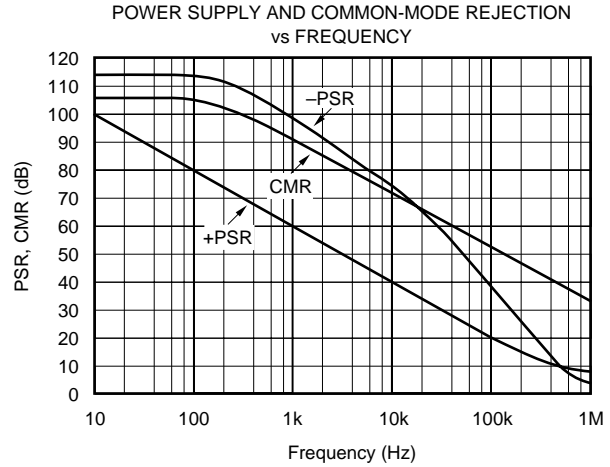
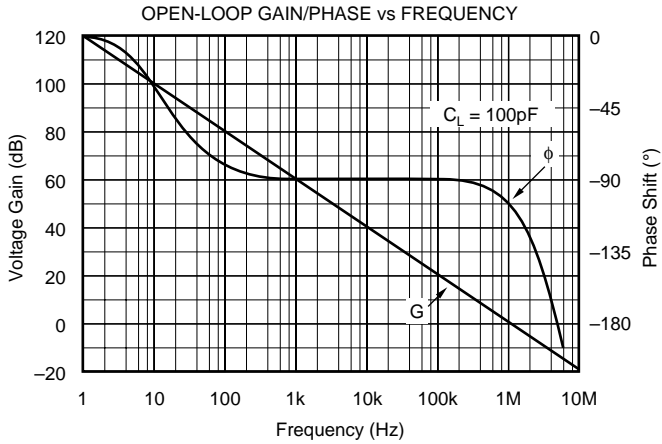
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITION	OPA130PA, UA OPA2130PA, UA OPA4130PA, UA			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature ⁽¹⁾ vs Power Supply Channel Separation (dual and quad)	Operating Temperature Range $V_S = \pm 2.25\text{V to } \pm 18\text{V}$		± 0.2 ± 2 2 0.3	± 1 ± 10 20	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
INPUT BIAS CURRENT⁽²⁾ Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		See Typical Characteristics $+5$ ± 2 ± 20 ± 20		pA pA
NOISE Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			30 18 16 16 4		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range, Positive Negative Common-Mode Rejection	$V_{CM} = -13\text{V to } +13\text{V}$	$(V+)-2$ $(V-)+2$ 90	$(V+)-1.5$ $(V-)+1.2$ 105		V V dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = -13\text{V to } +13\text{V}$		$10^{13} \parallel 1$ $10^{13} \parallel 3$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-loop Voltage Gain	$V_O = -13.8\text{V to } +13\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = -13\text{V to } +12\text{V}$	120 120	135 135		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	$G = 1$, 10V Step, $C_L = 100\text{pF}$ $G = 1$, 10V Step, $C_L = 100\text{pF}$ $G = 1$, $V_{IN} = \pm 15\text{V}$ 1kHz, $G = 1$, $V_O = 3.5\text{Vrms}$		1 2 5.5 7 2 0.0003		MHz V/ μs μs μs μs %
OUTPUT Voltage Output, Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation)	$R_L = 2\text{k}\Omega$ $R_L = 2\text{k}\Omega$	$(V+)-2$ $(V-)+1.2$ $(V+)-3$ $(V-)+2$	$(V+)-1.5$ $(V-)+1$ $(V+)-2.5$ $(V-)+1.5$ ± 18 10		V V V V mA nF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	± 2.25	± 15 ± 530	± 18 ± 650	V V μA
TEMPERATURE RANGE Operating Range Storage Thermal Resistance, θ_{JA} DIP-8 SO-8 Surface-Mount DIP-14 SO-14 Surface-Mount		-40 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Ensured by wafer test. (2) High-speed test at $T_J = 25^\circ\text{C}$.

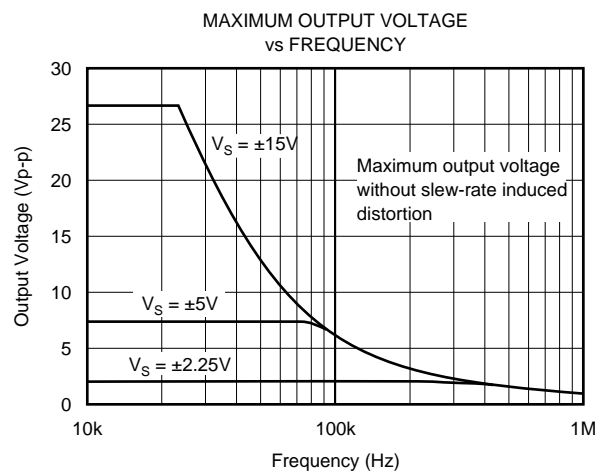
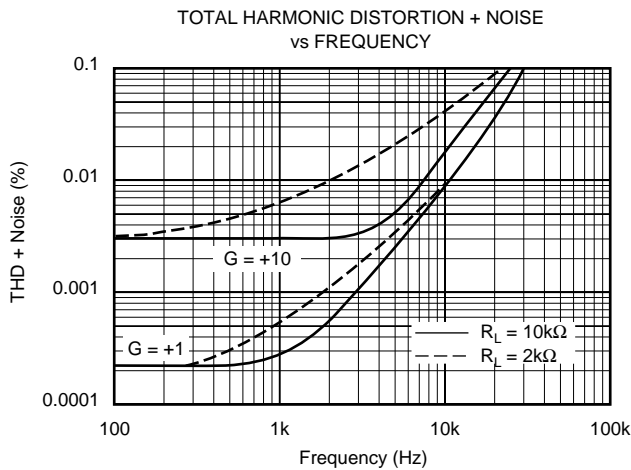
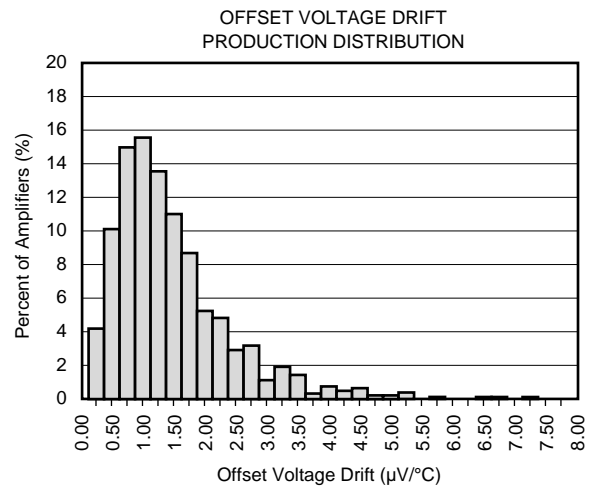
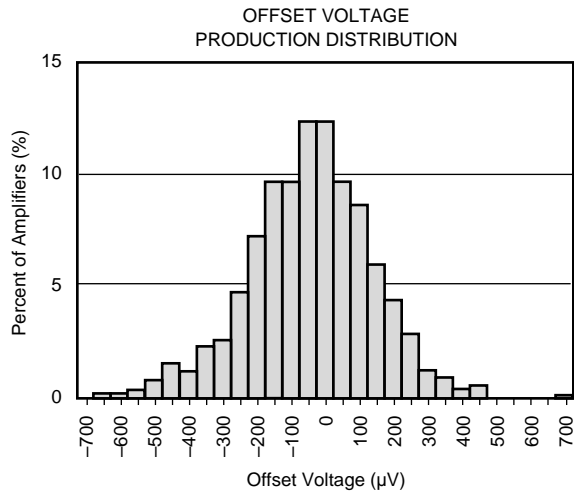
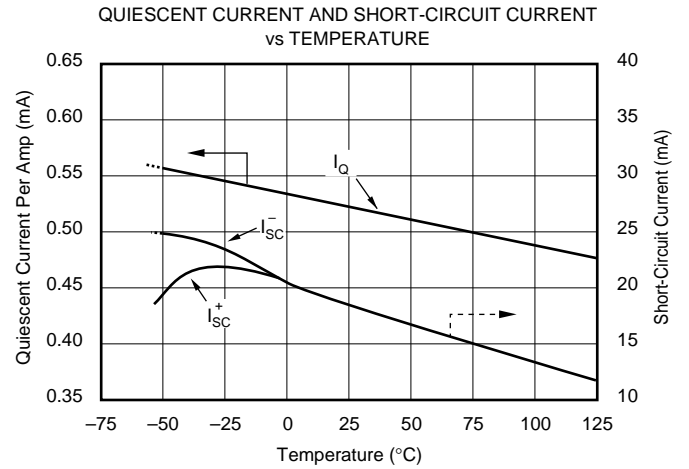
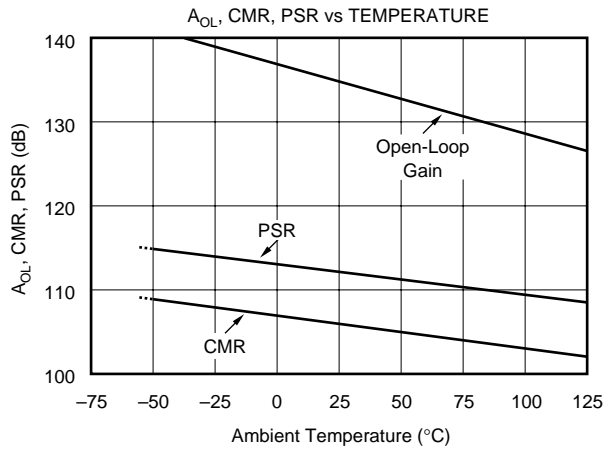
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

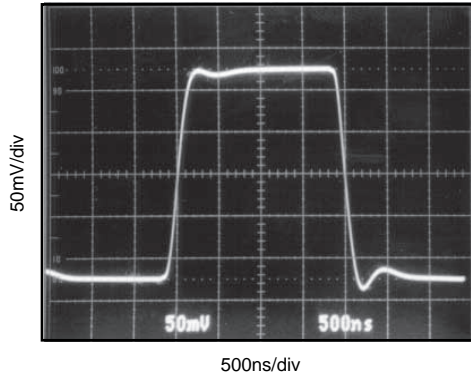
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.



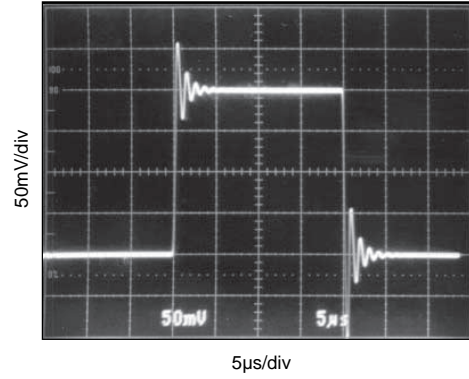
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.

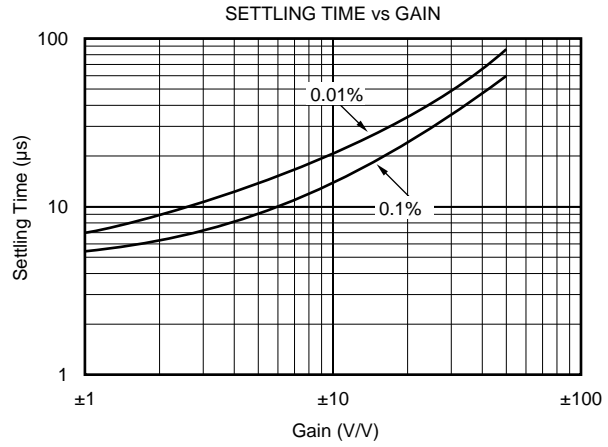
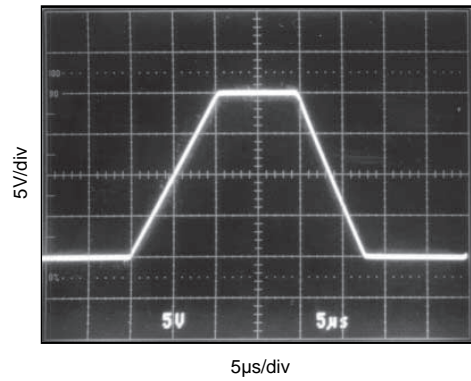
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$



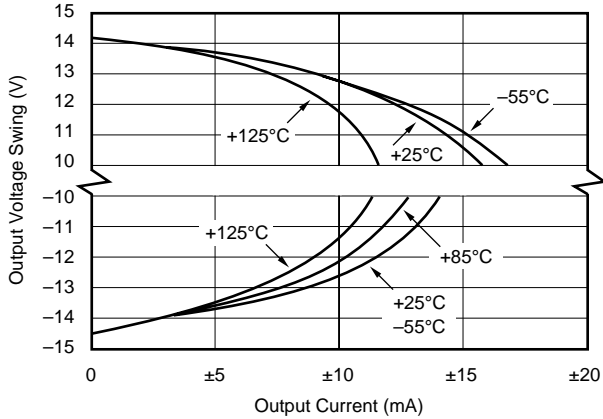
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 1000\text{pF}$



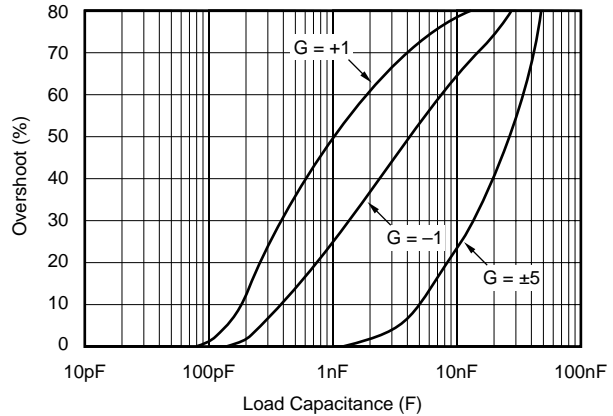
LARGE-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from $\pm 2.25\text{V}$ to $\pm 18\text{V}$ with excellent performance. Although specifications are production tested with $\pm 15\text{V}$ supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

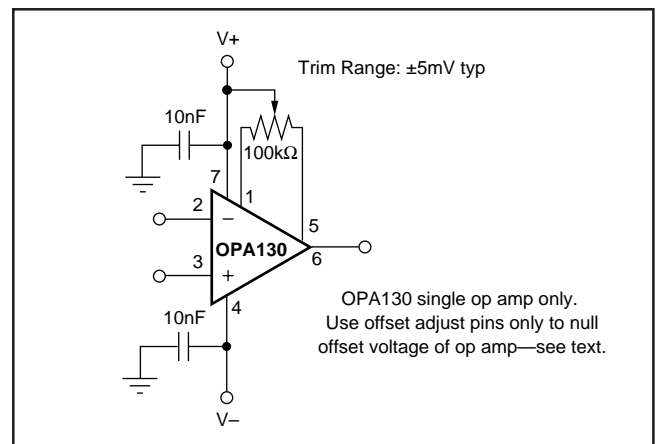


FIGURE 1. OPA130 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the Typical Characteristic curve *Input Bias Current vs Temperature*.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA130. See the Typical Characteristic curve *Input Bias Current vs Common-Mode Voltage*.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA130PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA130UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA130UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA130UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA130UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA2130PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA2130UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA2130UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA2130UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA2130UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA4130PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
OPA4130UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4130UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4130UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4130UAE4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the

accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4130UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

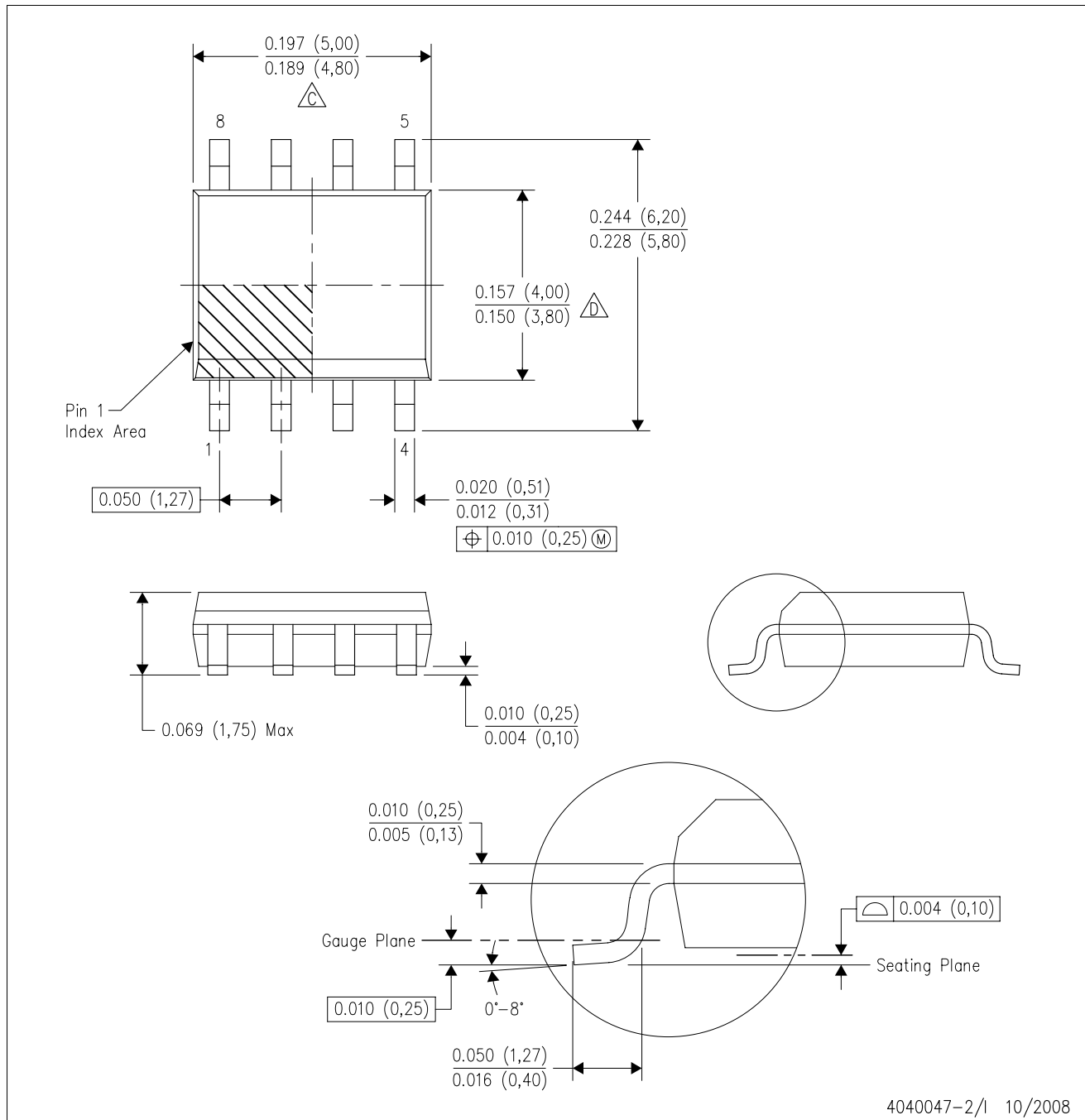


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA130UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA2130UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA4130UA/2K5	SOIC	D	14	2500	346.0	346.0	33.0

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated